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[Toshiba's Double Tunneling - The Quest for 100 Gb Flash Storage](#)

The new technology will be the cornerstone of huge-capacity Flash chips

Toshiba unveiled on Wednesday that they have developed a new design process that will become a key component in building high capacity Flash storage devices. This approach is named double-tunnel layer technology and it involves using a thin layer of silicon nano-crystals that stores information between a pair of tunnel oxide layers. Apart from the sandwich structure, there is a nitride layer that actually holds the electrons that record the cell's single data bit. These oxide coatings are meant to control the flow of electricity in and out of the silicon. The tunnel is one nanometer thick and allows for a smaller manufacturing process, namely the 10-nanometer standard. The technology is what the company calls the SONOS (Silicon Oxide Nitride Oxide Semiconductor) and is a revised version of Toshiba's older technology. The memory density is highly improved, which means that the same surface can hold up a much larger amount of data than the previous version. The read and write speeds have been dramatically improved. The memory elements have to be selected for the highest electrical purity, so that the tunnel process would allow storing about 100 gigabits (12.5 gigabytes) on a single-layer chip. Unfortunately, this technology is under perfecting and there are no working samples yet. Today's technology allows for chip manufacturing at 65-nanometer nodes or larger, but there is some progress made for shifting the manufacturing at lower nodes: 50nm, then 45nm and 32nm. Current common NAND flash memory to be found in consumer-electronics is built using a 16 gigabit process. In order to achieve higher storage capacities, manufacturers usually link multiple standard chips or chip stacks. NAND Flash memory generations have advanced on an yearly pace due to miniaturizing and shifting to a lower fabrication node. When switching on a lower architecture, both memory density and storage capacity increase. It seems that the technology can not go beyond the 10-nanometer limit, since the "Floating Gate" Flash designs are expected to become impractical.