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The new technology can easily be implemented into the manufacturers' production lines
Tom's Hardware

[How About Some Multi-Core RAM Memory?](#)

The new technology has some drawbacks, but promises a lot

Although it has suffered some dramatic functional improvements over the time, such as increased size or frequency, the RAM memory did not undergo the major change of parallel execution (as CPUs did). Memory has stuck to the same old architecture as in its early days, but things are about to change as parallel access to memory chips has kicked in. Joseph Ashwood, an independent security analyst claims to have outlined a revolutionary technology to unleash the power of parallel access to bit cells on memory chips. This new technology is called the "Ashwood architecture" and uses an integrated smart controller next to the memory array of the chip. This controller provides parallel access to the array for multiple concurrent processes. "We have a new way of assembling the memory, with a few new elements I was led to by my experience with cryptography. I am basically applying very deep cryptographic techniques to memory architecture, resulting in a unique new design that is very fast and compact. Bringing in these new elements enables a lot of good things, especially concurrency, permitting hundreds of simultaneous memory operations," said Ashwood. The cryptanalyst went to JoAnne Leff, founder of J.L. Associates in order to get representation during the licensing of the technology. However, she was skeptical regarding its functionality, so she sent the design to the Carnegie Mellon University for confirmation. However, it seems that the design is working and can be translated into a practical model. "We were skeptical, of course, but Carnegie Mellon confirmed for us that the Ashwood memory architecture really is a breakthrough in memory design," said Leff. "Now we want to license it to all major players involved in the applications of this technology, not only to improve the performance of individual memory chips, but also to give users fast, parallel access to solid-state drives." The technology comes with a "but": apart from its being a theoretical design that has not been transposed into a working unit, the new architecture slows down memory access times to the individual memory cells, as a result of multiple access channels. The technology can be perfected, but everything depends on whether it will be licensed or not. However, if the answer is positive, it may open the doors to a new era in parallel computing.