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AMD will leave 8 cores behind and will jump in the 12-core bandwagon instead
AMD

[AMD Ditches 8 Cores, Goes Straight for 12-Core Servers](#)

6-core processors are still on the roadmap

The last roadmap update from AMD unveiled new information regarding the company's upcoming server-oriented processors. Despite the fact that AMD previously informed the market about its plans regarding the [Hydra native 8-core architecture](#), the chip manufacturer will ditch it in favor of 12-core counterparts. According to AMD's vice president Randy Allen, the company will deliver both single-die, 6-core and dual-die, 12-core Opteron processors by 2012. Moreover, the new chips will be built using the 45-nanometer process that will be premiered in the Shanghai quad-core processor, expected later this year. Intel will soon start shipping its Nehalem micro-architecture and AMD seems ready to face competition with the 45-nanometer Shanghai cores, although Intel has long since switched to 45-nanometer High-K metal gating. The Shanghai chip is based on the Barcelona silicon with a 45-nanometer refresh, which would bring increased performance at a lower energy cost. Allen also claims that the Shanghai parts will offer 20 percent more computing power than the existing Barcelona line-up. More than that, while Intel's Nehalem chips will ditch the LGA 775 socket for the LGA 1366 one (because of the integrated memory controller), AMD's Shanghai chip will preserve compatibility with the current Socket F (1207). The Shanghai chip is already sampling to AMD's selected partners and is slated to mass-release in early 2009, although production will ramp up later this year. Later next year, AMD will also release a single-die 6-core Socket F chip in the Istanbul family, but its core frequency is nothing to be proud of. The radical shift in terms of platform will take place with the advent of the "Maranello" architecture, that will work with the single-die, 6-core "Sao Paulo" chip (6 MB of L3 cache), as well as the dual-die 12-core "Magny Cours" processor with 12 MB of L3 cache. "The more cores you put in there, the slower you're going to have to run it within a fixed power envelope", said Allen. "If you're going to add additional cores, you have to be very convinced that the majority of applications you're running are going to be able to take advantage of those additional cores. If they aren't able to do so, you're actually taking a step backwards", he continued. Both the "Sao Paulo" and the "Magny Cours" chips will likely use a different socket layout and will be built on the 45-nanometer processing node. AMD plans to pair the processors with one of the in-house chipsets (RD890S and RD870S northbridges and the SB700S southbridge).