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The Magny-Cours chip will be built of two 6-core Sao Paolo processors
AMD

[AMD's 12-Core Magny-Cours Chip Sports Direct Connect Module](#)

Two 6-core Sao Paolo processors working as one

AMD's recently published CPU roadmap schedules the [12-core Magny-Cours processor](#) for a 2010 release date. However, despite the fact that the chip is in its early design stage, information about the 12-core behemoth already started to emerge on the specialized forums. While Intel is currently using the MCM (multi-chip module) technology to connect two dual-core architectures in its quad-core processors, AMD plans to achieve the 12-core chip using its home-brewed DCM (Direct Connect Module). Although the two technologies have similar approaches, the MCM makes heavy use of the northbridge chip. The DCM relies exclusively on HyperTransport to interconnect the cores, which dramatically reduces idle times. The 12-core Magny-Cours chip is in fact comprised of two six-core Sao Paolo processors, interconnected by a coherent HyperTransport link. The HyperTransport technology will bridge the two six-core parts and will allow them to work together as a 12-core monolithic structure. Moreover, the 12 cores will be able to share a large L3 cache pool of 12 MB that is in fact the result of two 6 MB level-3 caches. AMD has perfected the technology in such a way that the chip won't be able to identify that data is actually deposited in two L3 cache pools. Intel seems to be one step behind AMD, as its quad-core Yorkfield processor still has management issues and sees the two 6 MB of cache memory as two distinct entities. However, the 12-core silicon is still a future project. At the moment, AMD does not quite have a worthy opponent for Intel's upcoming 6-core Dunnington chip, expected to arrive in a few months. Intel showed the Dunnington CPU during the spring edition of the Intel Developer Forum and its capabilities looked pretty solid, except for the fact that it went belly up at the end of the demonstration.